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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,188	10/30/2000	Tom E. Burton	219.38762X00 (P9439)	5131

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EXAMINER	
DONAGHUE, LARRY D	
ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,188	BURTON ET AL.	
	Examiner	Art Unit	
	Larry D. Donaghue	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-35 and 41-47* is/are allowed.

6)☒ Claim(s) *1,2,13 and 23* is/are rejected.

7)☒ Claim(s) *3-12, 14-22 and 36-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-47 are presented for examination.

2. The art presented in response of 105 request have been made of record in this action, note attached PTO 892.

Claims 24-35 and 41-47 are allowed as the prior art of record fails to detail a Transmitter Header Hardware Assist (HWA) Mechanism configured to generate OpCode and Length fields for an outgoing data packet when an entire data packet is being assembled for transmission, via the serial interface so as to offload said Micro-Engine (ME) from having to build all data packets for data transfers.

3. **Claims 3-12, 14-22 and 36-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims although it would be obvious some type of hardware or functionality would be necessary to perform the operation claimed the express combination recited in the claims, is not.**

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 13 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by The applied reference has a common Inventor and Assignment with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As to claim 1, Leitner et al. taught host-fabric adapter installed at a host system for connecting to a switched fabric of a data network (120), comprising: a Micro-Engine (ME) arranged to establish connections and support data transfers via said switched fabric (710); a serial interface arranged to receive and transmit data packets from said switched fabric for data transfers (730); a host interface arranged to receive and transmit host data transfer requests, in the form of descriptors, from said host system for data transfers (712); a first-in/first-out (FIFO) interface arranged to receive and transmit data packets to/from said switched fabric via said serial interface (722), and incorporated therein a Receiver Header Hardware Assist (HWA) Mechanism configured to check header information

of incoming data packets host descriptors for header errors so as to offload said Micro-Engine (ME) from having to check for said header errors (col. 11, line 43-50). (see col. 9, line 36 – col. 11, line 58, for functions of elements 710,712, 730, 722).

As to claim 1, Leitner et al. taught said Receiver Header Hardware Assist (HWA) mechanism comprises: context registers loaded with context information pertaining to an incoming data packet (col. 11, line 10-25); header registers loaded with header information of the incoming data packet; and a processor arranged to execute header checks and comparisons of the header information and the context information and determine whether the incoming data packet is good (col. 11, line 43-50, note the processing unit and storage are inherent for the operation detailed in the reference).

6.

As to claim 13 Leitner et al. taught an address translation interface which provides an interface for address translation, and which is addressable by write data and system controls from said Micro-Engine (ME), via a system data bus and a system control bus (714); a context memory which provides an interface to a context manager, and which is addressable by write data and system controls from said Micro-Engine (ME), via said system data bus and said system control bus, for providing the necessary context for a work queue pair used for sending and receiving data packets; a local bus interface which provides an interface to a local bus (716), and which is addressable by write data and system controls from said Micro=Engine (ME) (710), via said system data bus and said system control bus, for supporting system accessible context connections and data transfers; and a completion queue/doorbell manager interface which provides an interface to completion queues, and doorbell and memory registration rules (720) , and which is addressable by write data and system controls from said Micro-Engine (ME), via said system data bus and said system control bus (see col. 10, lines 36 – col. 12, line 37 for functional details)

As to claim 23, Leitner et al taught said host interface, said serial interface, said FIFO interface and said Micro-Engine (ME) are configured in accordance with the "Virtual Interface (VI) Architecture Specification", the "Next Generation Input/Output (NGIO) Specification" and the "InfiniBand' Specification".

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gasbarro et al.	2002/00761450
Ward	6,937,611
Burton et al.	6,778,548
Johnson	6,591,310
Latif et al.	2003/0091037
Parthassarathy et al.	6,831,916
Buonadonna et al.	An Implementation and Analysis of Virtual Interface Architecture

Patel et al.	A Model of Completion Queue Mechanisms using the Virtual Interface API
Cole et al.	High Speed Digital Transceivers: A Challenge for Manufactoring
Garcia et al.	Future I/O
Unknown,	An Analysis of VI Architecture Primitives in Support of parallell and Disrtibuted Communications

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larry D. Donaghue whose telephone number is 571-272-3962. The examiner can normally be reached on M-F 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).